

INFORMATION DISCLOSURE STATEMENT

Case Name & No.
Serial No.
Filing Date:
Group:

CHANG 7-20-10
2/IDS
e. Hillis
11-22-99

525 U.S. PTO
09/414226



U.S. PATENT DOCUMENTS

*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date
AA						
AB						

FOREIGN PATENT DOCUMENTS

Document Number	Date	Country	Class	Subclass	Translation
AC					
AD					

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

DNK	AE	Chatterjee et al., "IEEE", Sub-100nm Gate Length Metal Gate NMOS Transistors Fabricated by a Replacement Gate Process, pages 821-824, 1997.
DNK	AF	Taur et al., "IEEE", 25nm CMOS Design Consideration, pages 789-792, 1998.
DNK	AG	Chatterjee et al., "IEEE", CMOS Metal Replacement Gate Transistors Using Tantalum Pentoxide Gate Insulator, pages 777-780, 1998.
	AH	
	AI	
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EXAMINER

Donghee Kang

DATE CONSIDERED

6-11-01

*Examiner r: Initial if reference considered, whether or not citation is in conformance with MPEP 609: Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.